EAST - [jig.wsp:1]

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Active
L1: (1634) STI.clm. or (shallow adj trench adj isolation).clm.
L2: (83) 1 and (second adj (mask or resist or photoresist)).clm.
L3: (70) 2 and (etch$3.clm. or pattern$3.clm.)
L4: (26) 3 and (etch$3 near (mask or photoresist or resist))
L5: (9) 3 and (remov$3 near (second adj mask))
Failed

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DBs | USPAT; US-PGPUB | Plurals

Default operator: OR | Highlight all hit terms initially

3 and (remov$3 near (second adj mask))

Basic form | Boolean form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3	4	5	Ima
1	☐	☐	US 20040005752 A1	20040108	19	voltage threshold and low	438/217			Helm, Mark et al.	☑	☐	☐	☐	☐	☐	☐	US 200
2	☐	☐	US 20030124813 A1	20030703	9	Method of fabricating shallow trench isolation	438/400	257/E21.232; 257/E21.244;		Lee, Shyh-Dar	☑	☐	☐	☐	☐	☐	☐	US 200
3	☐	☐	US 20030119248 A1	20030626	13	Method of fabricating dual threshold voltage n-channel	438/217	257/E21.633; 438/289;		Mistry, Kaizad R. et al.	☑	☐	☐	☐	☐	☐	☐	US 200
4	☐	☐	US 20030094659 A1	20030522	13	METHOD OF FABRICATING DUAL THRESHOLD VOLTAGE N-CHANNEL	257/369	257/374; 257/391;		MISTRY, KAIZAD R. et al.	☑	☐	☐	☐	☐	☐	☐	US 200
5	☐	☑	US 20020016035 A1	20020207	17	Method for making deep trench capacitors for DRAMs	438/243	438/386		Wu, Chao-Chueh et al.	☑	☐	☐	☐	☐	☐	☐	US 200
6	☐	☐	US 6475894 B1	20021105	18	Process for fabricating a floating gate of a flash mem	438/593	257/E21.209; 257/E21.68;		Huang, Chung-Lin et al.	☑	☐	☐	☐	☐	☐	☐	US 6
7	☐	☑	US 6323092 B1	20011127	8	Method for forming a shallow trench isolation	438/296	257/E21.548; 438/404;		Lee, Hao-Ming	☑	☐	☐	☐	☐	☐	☐	US 6
8	☐	☐	US 6281069 B1	20010828	10	Method for forming deep trench capacitor under a sha	438/248	257/E21.653; 438/249;		Wu, Der-Yuan et al.	☑	☐	☐	☐	☐	☐	☐	US 6
9	☐	☐	US 6245635 B1	20010612	18	Method of fabricating shallow trench isolation	438/407	257/E21.548; 438/423;		Lee, Ellis	☑	☐	☐	☐	☐	☐	☐	US 6

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